REMARKS

Favorable reconsideration of this application is respectfully requested.

Claims 1-20 are pending in this application. Claims 17 and 20 have been withdrawn from consideration. Claims 1 and 2 have been amended to remove unnecessary parenthetical expressions of well-known parameters without the introduction of any new matter.

In the outstanding Official Action, Claims 1-16, 18, and 19 were rejected under the first paragraph of 35 U.S.C. §112 as failing to satisfy the enablement requirement therein, and Claims 1-5 and 18 were rejected under 35 U.S.C. §103(a) as being unpatentable over Iwamatsu et al (clarified at the discussion of August 16, 2000 to be the 1995 article entitled "*High-Speed 0.5μm SOI 1/8 Frequency Divider with Body-Fixed Structure for Wide Range of Applications*," hereinafter Iwamatsu) in view of Hwang et al (U.S. Patent No. 4,443,930, hereinafter Hwang).

Initially, Applicants acknowledge with gratitude the personal interview granted to Applicants' representative on August 16, 2000 by the Examiner. During this interview, the Examiner clarified that the reliance on "Iwamatsu et al" was intended as reliance on the Iwamatsu et al 1995 article entitled "*High-Speed 0.5μm SOI 1/8 Frequency Divider with Body-Fixed Structure for Wide Range of Applications*."

In addition to clarifying which of the "Iwamatsu et al" articles was intended in the Action, the rejection under the first paragraph of 35 U.S.C. §112 was discussed in terms of apparent conflict with the directives set forth in MPEP §2164.02 and §2164.04 and the case law noted therein. In this regard, applicants' representative pointed out that the statement of the rejection and reasons offered at page 3 of the Action seemed to state that the frequency range of greater than 500 MHz (Claim 1) and signal propagation delay time of less than 50 ps

(Claim 2) were not considered as enabled because they did "not appear to correspond to devices that have actually been made." However, as pointed out during the discussion there is no requirement that any device must be physically made as a condition precedent to enablement and that it was well established that the lack of a working example could not serve as the sole basis for a rejection under the first paragraph of 35 U.S.C. §112.

With respect to there being no absolute requirement for disclosure of a working example, Applicants' representative first pointed to MPEP §2164.02 which unmistakably indicates that compliance with the first paragraph of 35 U.S.C. §112 does not turn on whether disclosed examples are "working" or "prophetic." In addition, this section of the MPEP cites Gould v. Quigg, 822 F.2d 1074, 1078, 3 USPQ2d 1302, 1304 (Fed. Cir. 1987) as holding that "The mere fact that something has not previously been done clearly is not, in itself, a sufficient basis for rejecting all applications purporting to disclose how to do it." (Quoting In re Chilowsky, 229 F.2d 457, 461, 108 USPQ 321, 325 (CCPA 1956)). This section goes on to note that the lack of a working example cannot alone be the basis of a valid rejection under the first paragraph of 35 U.S.C. §112 ("In other words, lack of working examples or lack of evidence that the claimed invention works as described should never be the sole reason for rejecting the claimed invention on the grounds of lack of enablement.").

The examiner indicated that her concern was that there might be other conditions present that would prevent operations at frequencies greater than 500 MHz (Claim 1) or with a signal propagation delay time of less than 50 ps (Claim 2) and that this could not be known unless the devices were actually built instead of simulated as indicated, for example, in the sentence bridging pages 19 and 20 of the specification as to the use of a clock operating frequency of not less than 500 MHz. However, MPEP §2164.04 notes that In re Wright, 999

F. 2d 1557, 1562, 27 USPQ2d 1510, 1513 (Fed. Cir. 1993) requires that the examiner must meet the initial burden of establishing a reasonable basis to question the enablement provided for the claimed invention. The mere existence of doubt as to other conditions that might be present is not seen to comply with the requirements of In re Marzocchi, 169 USPQ 367, 369-370 (CCPA 1971):

> The only relevant concern of the Patent Office under these circumstances should be over the truth of any such assertion. The first paragraph of § 112 requires nothing more than objective enablement. How such a teaching is set forth, either by the use of illustrative examples or by broad terminology, is of no importance.
>
> As a matter of Patent Office practice, then, a specification disclosure which contains a teaching of the manner and process of making and using the invention in terms which correspond in scope to those used in describing and defining the subject matter sought to be patented must be taken as in compliance with the enabling requirement of the first paragraph of § 112 unless there is reason to doubt the objective truth of the statements contained therein which must be relied on for enabling support. Assuming that sufficient reason for such doubt does exist, a rejection for failure to teach how to make and/or use will be proper on that basis; such a rejection can be overcome by suitable proofs indicating that the teaching contained in the specification is truly enabling.
>
> * * * it is incumbent upon the Patent Office, whenever a rejection on this basis is made, to explain why it doubts the truth or accuracy of any statement in a supporting disclosure and to back up assertions of its own with acceptable evidence or reasoning which is inconsistent with the contested statement. Otherwise, there would be no need for the applicant to go to the trouble and expense of supporting his presumptively accurate disclosure. [Emphasis in original and footnote deleted.]

There is no basis for the examiner's apparent belief that the first paragraph of 35 U.S.C. §112 requires that a specification present absolute evidence to convince persons skilled in the art that the assertions therein are correct. See, e.g., In re Robins, 166 USPQ 552, 556 (CCPA 1970). Mere doubts are clearly not the required showing as to some technical basis for believing that the simulations performed are insufficient under the circumstances

here.

In addition, and as noted at the discussion of August 16, 2000, the relied upon Iwamatsu et al 1995 article entitled "*High-Speed 0.5μm SOI 1/8 Frequency Divider with Body-Fixed Structure for Wide Range of Applications*" establishes that the examiner's concern that the frequency range of greater than 500 MHz (Claim 1) and signal propagation delay time of less than 50 ps (Claim 2) did "not appear to correspond to devices that have actually been made" was clearly misplaced. Note the statement at page 575 under the heading "Experimental" as to CMOS transistor fabrication and Fig. 8 showing both bulk and body-fixed operation at above .5 Ghz. As was explained at page 21 of the specification, for example, the present invention is not based on simply providing devices that can be operated at frequencies above 500 MHz, it is to provide methods to design and reliably produce stable devices without having to rely on trial and error which was the previous method used.

The examiner further indicated concern with the statement that the designing was to be made as to any frequency greater than 500 MHz with no upper limit specified and recent court decisions not specifically identified. Before such decisions can be discussed they must be cited. To the extent the examiner is suggesting that she believes that Claims 1 or 2 violate the first paragraph of 35 U.S.C. §112 because enablement is not commensurate with the scope of the claims, this contention is not supported by the discussion in MPEP §2164.08 and the Fisher decision cited there (166 USPQ 18, 24 (CCPA 1970)). Moreover, MPEP §2164.02 further makes it clear that the mere lack of a working example cannot be the sole reason for a rejection based on the claims being broader than the enabling disclosure.

In any event, when considering that the only question raised in the outstanding Action is the lack of the device actually having been made and that this alone is never alone a reason

that is sufficient to reject claims under the first paragraph of 35 U.S.C. §112 along with the above noted evidence of record of the actual making of a device operating at a frequency greater than 500 MHz and time delays of less than 50 ps, it is respectfully urged that the outstanding rejection based on the first paragraph of 35 U.S.C. §112 is improper and should be withdrawn.

Before turning to the outstanding rejection for obviousness, it is believed that a brief review of the present invention would be helpful. In this respect, the present invention is directed to a method of designing a semiconductor device having an SOI structure in which the operating speed is not effected so as to become unstable at frequencies greater than 500 MHz. In this respect, the design criteria is the forming of such an SOI structure which satisfies the equation $R \cdot C \cdot f < 1$ where f, R, and C are specifically defined in both the claims and specification as noted during the discussion of August 16, 2000.

In another aspect of the invention, an MOS transistor having an SOI structure is formed using a designing method in which a layout pattern of the MOS transistor is determined to satisfy the expression $(R \cdot C)/td < 1$ where $td \leq 50$ ps, with the parameters td, R, and C again having specific claim and disclosure definitions as also noted in the discussion of August 16, 2000.

In addition to the method of making such devices, the devices made by these methods are also claimed.

Turning to the outstanding rejection of Claims 1-5 and 18 under 35 U.S.C. §103 as unpatentable over Iwamatsu in view of Hwang, it is first noted that the action acknowledges that Iwamatsu does not teach how to design the disclosed SOI structure so that it can reliably provide the stable high frequency operation of the device of Claim 1, for example. To

whatever extent the device of Iwamatsu has a body region and a fixed potential transmission path extending between it to a body contact, there is no way to know the resistance of this transmission path, the gate capacitance of the MOS transistor, much less that R·C·f (apparently 2.5 GHz) is less than 1. In order to suggest that the artisan would have made R·C·f (f≥ 500MHz) less than 1, the Action relies upon the teaching of Hwang at column 1, lines 24-40 as teaching that the RC time delay of a transmission path should be less than the intrinsic device delay which is noted to be related to gate width. What the action fails to note is the actual teaching of Hwang at this location is that a long polysilicon line has a resistance and capacitance and the object is to maintain the RC time delay of this long polysilicon line at a desired value, which has nothing to do with the "fixed potential path" recited in Claims 1 and 2. Thus it in is stated in Hwang that the resistance of a 1000 μm line would cause a delay time of nearly 20 ns which is significantly greater than that of the device but no such long polysilicon lines are taught or are of any concern in Iwamatsu nor can such long polysilicon lines be reasonably equated with the "fixed potential path"of Claims 1 and 2.

If the artisan where to reasonably use the teachings of Hwang to design the device of Iwamatsu, he would merely be concerned with the R·C time constant of the gate electrode or a wiring line and not with the resistance of the "fixed potential transmission path" defined in Claims 1 and 2. Moreover, absent the present disclosure, there would exist no reason to believe that this resistance of a "fixed potential transmission path" and MOS gate capacitance have any effect on stability as to operating at frequencies above 500 MHz as Claim 1 requires.

Similarly, with respect to independent Claim 2, the resistance of concern is again that of a "fixed potential transmission path" extending from at least one body contact to a body

region as defined above and not the resistance of a long polysilicon line. Moreover, the capacitance is again that of the gate of the MOS transistor and not that associated with a long polysilicon line and there is no hint in the references that any particular relationship of this MOS gate capacitance and the resistance of the "fixed potential transmission path" defined above should be related to signal propagation delay time in any particular fashion, at least not outside of Applicants' disclosure which cannot be used.

Finally, it is noted that the criticality of the designing of the device to achieve particular delay times and a high speed operating frequency so that the designed device can be operate with stability has been adequately set forth in the specification. Consequently, the allegation as to the lack of a showing of criticality is not understood.

Substantially the same arguments made above as to Claims 1 and 2 apply equally to Claims 3 and 5 which ultimately depend on Claim 1 and Claims 4 and 18 which ultimately depend on Claim 2. In addition, each of these dependent claims add further features to the base claims which are neither taught nor disclosed by the applied references considered alone or in any proper combination. Accordingly, the rejections of Claims 3-5 and 18 are traversed for the reasons presented as to the base claims as well as because of these additional features which are neither taught nor described by the references.

Since no other issues are believed to be outstanding in the present application, it is believed to be clearly in condition for formal allowance. Consequently, an early and favorable action to that effect is earnestly and respectfully requested.

Respectfully submitted,

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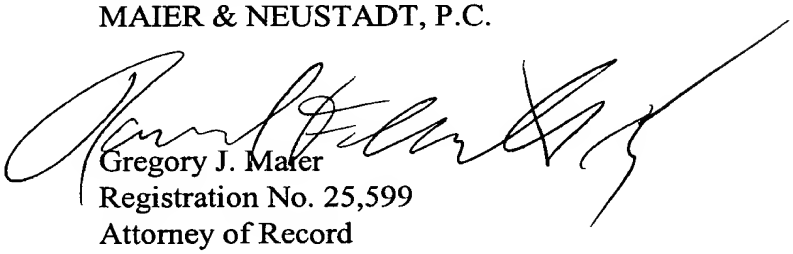

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